REMARKS

Prior to the present response, claims 1 and 3-20 were pending in the present application, and remain pending after the present response. Reconsideration and allowance of outstanding claims 1 and 3-20 in view of the following remarks are respectfully requested.

A. Rejection of Claims 1 and 3-20 under 35 USC §103(a)

The Examiner has rejected claims 1 and 3-20 under 35 USC §103(a) as being unpatentable over U.S. Patent Application Publication Number US 2004/0031699 A1 to Shoji ("Shoji") in view of U.S. Patent Number 5,175,472 to Johnson, Jr. et al. ("Johnson"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claims 1 and 11, is patentably distinguishable over Shoji and Johnson, either singly or in combination.

The present invention is directed to circuit for detecting arcing in an etch tool during wafer processing. As defined by independent claims 1 and 11, the present invention includes, among other things, an electrostatic chuck ("ESC") input for receiving a first signal that indicates a magnitude of a chuck current passing through a chuck holding a wafer in the etch tool. In addition, the present invention includes a VRF input for receiving a second signal from the etch tool, which indicates a RF voltage of a plasma. Furthermore, the present invention includes a unique arc detect output for indicating whether a true arc event has occurred.

In one embodiment of the present invention, as shown in Figure 2, ESC input 212 is connected to a signal input of ESC signal level detector 218. ESC signal level detector 218 can output a signal when an arc event is detected at the signal input of ESC signal level detector 218. ESC signal level detector 218, however, does not distinguish between a wafer arc event and chucking and de-chucking spikes at ESC input 212. Nonetheless, as seen in Figure 3, the present invention advantageously ignores chucking and de-chucking spikes similar to chucking spike 374 and de-chucking spike 382.

For example, VRF signal level detector 250 can be configured to output a signal, such as a logical one, when plasma 108 in etch tool 102 in Figure 1 has been activated. See, for example, page 11, lines 7-9. Moreover, power on delay module 258 can be set to delay a signal provided at the output of VRF signal level detector 250 so as to prevent the output signal received from the output of VRF signal level detector 250 from reaching the second input of gate 226 during a wafer chucking procedure. See, for example, page 12, lines 2-9. Therefore, power-on delay module 258 can prevent VRF signal level detector 250 from sending a logical one to gate 226 for an exemplary period of two seconds required for a chucking procedure, and thus the signal provided at the output of gate 226 will advantageously ignore occurrence of a chucking or de-chucking spike. See, for example, page 15, line 6-9. Thus, the present invention uniquely and advantageously ignores spikes that occur during chucking and de-chucking procedures and provides a desired output only when a verified wafer arc event occurs. See, for example, the present application, page 8, lines 11-14.

The Examiner asserts that by including the limitation in independent claim 1 which recites "wherein said arc detect output does not indicate an occurrence of a chucking spike and a de-chucking spike in said etch tool," that "Applicants are merely claiming the obvious, which is the failure of integrated circuits occurring and no output of a signal will result." Present office action, page 2, paragraph 4. Applicants respectfully disagree. A critical feature of the present invention is that arc detect circuit 110 in Figure 1 "can be configured to ignore spikes that occur during chucking and de-chucking procedures, and to provide a specified output *only* when a verified wafer arc event occurs." Present application, page 8, lines 11-14 (emphasis added). In other words, chucking and de-chucking procedures cause spikes in the chuck current signal that resemble spikes caused by wafer arcing, where the present invention can be configured to selectively ignore chucking and de-chucking spikes while providing a specified output only when a verified wafer arc event occurs. See the present application, page 8, lines 10-11.

Applicants, therefore, respectfully submit that the present invention's ability to ignore chucking and de-chucking spikes cannot merely be the obvious result of "a failed circuit" as the Examiner suggests, because in such a case the present invention would not be able to provide a specified output *only* when a verified wafer arc event occurs. More specifically, a failed circuit would not only result in ignoring chucking and de-chucking spikes, but would also result in the ignoring of verified wafer arc events as well. Thus, Applicants respectfully submit that the novel features of the present invention, which include the present invention's ability to selectively ignore chucking and de-chucking

spikes while providing an output for verified wafer arc events, cannot be achieved simply by way of a failed circuit.

In contrast to the present invention, the disclosure in Shoji does not teach, disclose, or suggest "an arc detect output indicating whether an arc event has occurred, wherein said arc detect output does not indicate an occurrence of a chucking spike and a de-chucking spike in said etch tool," as required by independent claim 1, because the disclosure in Shoji "is configured to detect arcing that occurs during the entire time the substrate 102 is processed in the system 100, including chucking and dechucking." Shoji, paragraph 28, lines 15-18 (emphasis added). As such, Shoji also fails to teach, disclose, or suggest "an arc detect output indicating whether an arc event has occurred; wherein said circuit is configured to prevent said arc detect output from indicating an occurrence of a chucking spike and a de-chucking spike in said etch tool," as required by independent claim 11.

Johnson, in contrast, discloses a plasma power monitor that enables sensing voltage and current at or near the RF load. See, for example, Johnson, column 1, lines 25-26 and lines 44-45. Johnson, however, fails to address the novelty of the present invention in that the disclosure in Johnson ignores spurious arcing events. Therefore, even if Johnson's Sample and Hold Frequency Converter 14 were equivalent to the VRF input of the present application (and Applicants disagree that the two are equivalents) as the Examiner suggests, Johnson does not cure the deficiencies of Shoji. For example, neither Shoji nor Johnson discloses or suggests the desirability of, or the mechanism used

for, screening spurious "acring events" such as chucking and de-chucking spikes, as disclosed and claimed by the present invetion. The same can be said about A/DC 70, 55, 63, or 56 of Johnson.

Accordingly, Johnson cannot be combined with Shoji to achieve the present invention because Johnson does not make any reference to providing an arc detect output which ignores occurrence of chucking and de-chucking spikes in an etch tool. Thus, Shoji and Johnson, even if combined, do not achieve the present invention as defined by independent claims 1 and 11.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by independent claims 1 and 11, is not taught, disclosed, or suggested by the art of record. Thus, independent claims 1 and 11 are patentably distinguishable over the art of record. As such, the claims depending from independent claims 1 and 11 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 11, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1 and 3-20 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing

reasons, an early allowance Notice of Allowance directed to all claims 1 and 3-20 remaining in the present application is respectfully requested.

Respectfully Submitted,
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